REMARKS

Claims 1-14 are pending. Claims 1, 5, 9, 10 and 11 are amended. Reconsideration and allowance based on the below comments are respectfully requested.

The Office Action rejections claims 1, 4, 5, 8, 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over Ooi (US 6,362,913) in view of applicants' admitted prior art; claims 2 and 6 under 35 U.S.C. §103(a) as being unpatentable over Ooi, applicants' admitted art and Miyamoto, et al. (US 6,559,996); claims 3 and 7 under 35 U.S.C. §103(a) as being unpatentable over Ooi, applicants' admitted prior art and Jabr (US 6,229,632) and claims 11-14 under 35 U.S.C. §103(a) as being unpatentable over Ooi, applicants' admitted prior art and Ishihara (US 5,557,648). These rejections are respectfully traversed.

In applicants' admitted prior art, modulation is carried our in a condition where a modulation factor $\beta = \pi$, and an initial phase δ is set to $\delta = \pi/2$. Judging from the waveform in Ooi, it appears that the modulation factor β and the initial phase δ are the same as in applicants' admitted prior art. See page 2, lines 17-23. In contrast, the Mach-Zender optical modulator in embodiments of the present invention carries out modulation in a condition where a modulation factor β is set to $\beta = 2\pi$, and an initial phase δ is set as $\delta = 0$, and outputs an output optical signal having a repetitive frequency 2fc (Hz) by a driving signal or repetitive frequency fc (Hz). See page 16, lines 19 – page 17, lines 3. The Mach-Zender optical modulator is set in accordance with the above in order to achieve the features of the embodiments of the present invention.

Applicants' respectfully submit that applicants' admitted prior art teaches contrary to the features of applicants' embodiments as discussed directly above. Further, applicants' respectfully submit that Ooi also fails to teach or suggest these features. Thus, the modulation

factor β and phase δ as recited in applicants' independent claims 1, 5, 9, 10 and 11 are not taught by the combination of applicants' admitted prior art and Ooi.

Thus, the combination applicants' admitted prior art and Ooi fail to teach or suggest, *inter alia*, modulation factor β of the Mach-Zender optical modulator is set to $\beta = 2\pi$, and initial phase δ of the Mach-Zender optical modulator is set as $\delta = 0$ for outputting the optical pulse string having a frequency two times that of a driving signal (fc), as recited in independent claims 1, 5, 9, 10 and 11.

Further, Ooi teaches a system in which an optical modulator is driven by a modulator driving voltage signal. A low frequency signal is superimposed on the modulator driving voltage signal. The output of the modulator is then processed through a combination of a photodiode 57a, amplifying circuit 57b, phase comparator 57c and low pass filter 57d. Processing the output signal through this combination allows for the detection of the drift of the operating point of the optical modulator. The bias voltage is then adjusted in accordance with the detected drift to control the operating point of the modulator. See column 14, lines 38-67 through column 15, lines 1-16.

The Office Action alleges that the detected drift in Ooi is an error signal that corresponds to the error signal as recited in applicants' claims. As recognized by the Office Action, the detected drift or alleged error signal, is not added to a bias voltage to create a controlled biased signal. The Office Action alleges that applicants' admitted prior art provides this teaching absent in Ooi. Applicants respectfully disagree.

Applicants' admitted prior art teaches a system in which a low pass signal derived from a synchronous detector circuit is added to a bias voltage. The added signal is then provided to an

optical modulator. The synchronous detector circuit includes a mixer 117, op amp 108 and low pass filter 109. In applicants' admitted prior art, an error signal is not added to the bias voltage. See Fig. 12, page 5, lines 3 to page 7.

In embodiments of applicants' invention, the signal part of an output signal is converted to an electrical signal, amplified and sent trough a band pass filter. The filtered signal is then processed by an error generator circuit 7. The error generating circuit includes a level detector 7a to detect a level of the frequency component of the signal, a CPU 7b and D/A converter 7c which generates an error signal that shows an error of the bias voltage. The error signal is then added to the bias voltage.

The embodiments of the present invention create an error signal derived from the filtered signal to obtain accurate error correction data to be added to the bias voltage. In contrast, applicants admitted prior art provides the filtered signal directly to the bias voltage.

Thus, the features of adding an error signal to the bias voltage as recited in claims 1, 5, 9, 10 and 11 of embodiments of the applicants' invention is not taught by Ooi or applicants' admitted prior art.

Therefore, the combination of Ooi and applicant's prior art fails to teach or suggest, *inter alia*, a bias voltage control unit which applies a bias voltage obtained as a result of addition of the bias voltage and voltage corresponding to the error signal to said optical modulator as recited in claim 1; a bias voltage control unit which applies a bias voltage as with an error signal, the bias voltage to said optical modulator, as recited in claim 5; applying a bias voltage obtained as a result of addition of the bias voltage and the voltage corresponding to the error signal to said

optical modulator, as recited in claim 9; and applying a bias voltage, added with the voltage corresponding to the error signal to said optical modulator as recited in claim 10.

Regarding claim 11, Ooi and applicants' admitted prior art have been combined with Ishihara's teachings. Ishihara teaches a phase lock loop circuit that contains a phase box date even for a consecutive identical bits data of input data. A variation of a phase comparator, low pass filter and frequency control terminal are used to maintain the phase lock state. However, Ishihara does not teach or suggest adding an error signal to a bias voltage as claimed.

Thus, Ishihara fails to make up for the deficiencies of Ooi and applicants' admitted prior art. Therefore, the combination of Ooi, applicant's admitted prior art and Ishihara fail to teach or suggest, *inter alia*, providing a control to generate the bias voltage, said bias voltage being generated from combining said error signal with a predetermined biased voltage; wherein said bias voltage being generated from combining said error signal with a predetermined biased voltage, wherein said bias voltage and said driving signal being input to drive the optical modulator, as recited in claim 11.

Further, applicants respectfully submit that one of ordinary skill in the art would not modify Ooi's system in view of applicants' admitted prior art. Applicants admitted prior art at best teaches adding a filtered signal to a biased voltage. Applicants' admitted prior art does not teach or suggest adding an error signal obtained from the filtered signal to the biased voltage as claimed. Further, the system of Ooi relies upon the detected drift to determine how to control the biased voltage. The addition of the detected drift to the bias voltage would not serve this purpose and in fact makes no practical sense. The detected drift merely indicates the direction of the drift. Adding the drift signal to a biased voltage would not compensate for bias error in Ooi's

system. It is the drift value itself and separately from the biased voltage that allows it to contribute to determining how to compensate the biased voltage. Thus, one of ordinary skill would not be motivated based on applicants' admitted prior art to add a signal to the biased voltage as suggested in applicants' admitted prior art.

Therefore, in view of the above, applicants respectfully submit Ooi, applicants' admitted prior art, Miyamoto, Jabr and Ishihara alone or in any combination fail to teach each and every feature of applicant's independent claims as required. Also, applicants respectfully submit that one of ordinary skill would not be motivated to combine the teachings of applicant's admitted prior art with Ooi as suggested in the Office Action. Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

Conclusion

For at least these reasons, it is respectfully submitted that claims 1-14 are distinguishable over the cited art. Favorable consideration and prompt allowance are earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Chad J. Billings (Reg. No. 48,917) at the telephone number of the undersigned below to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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